Claims

What is claimed is:

1. A method for forming a plurality of channels in or on a substrate, the method comprising:
   (a) depositing a first masking material on a substrate having a first region at a first level and a second region at a second level higher than the first level;
   (b) etching the first masking material from the substrate to produce a first sidewall extending from the substrate at an intersection of the first and second regions;
   (c) depositing, on the substrate, a second masking material different from the first mask material, the second masking material covering the first and second regions and the first sidewall;
   (d) etching the second masking material from the substrate to produce a second sidewall adjacent to the first sidewall, the first and second sidewalls having pitches on the order of nanometers;
   (e) repeating steps (a)-(d) a predetermined number of times to produce a plurality of adjacent nanometer-pitched sidewalls alternatingly formed of the first and second masking materials, the adjacent nanometer-pitched sidewalls forming a plurality of nanometer-pitched channels on the substrate.
2. The method of claim 1 comprising selectively etching one of the first and second masking materials from the substrate, leaving sidewalls formed of the masking material remaining on the substrate, the sidewalls being spaced from each other on the substrate by nanometer-scale dimensions and etching regions of the substrate between the sidewalls to form a plurality of first channels in the substrate spaced from each other by nanometer-scale dimensions.
3. The method of claim 2 wherein the substrate includes sidewalls between the channels having nanometer-scale dimensions.

4. The method of claim 1 wherein depositing a first masking material on a substrate includes depositing the first masking material on the substrate with the first degree of anisotropy and wherein etching the first masking material from the substrate includes etching the first masking material from the substrate with a second degree of anisotropy being different from the first degree of anisotropy.

5. The method of claim 4 wherein depositing and etching the first masking material from the substrate with different degrees of anisotropy includes depositing the first masking material with a greater thickness in the vertical direction at the intersection of the first and second regions of the substrate than the thickness of the first masking material in the first and second regions and uniformly etching the first masking material from the substrate in the vertical direction, thereby producing the first sidewall.

6. The method of claim 1 wherein etching the first and second masking material from the substrate includes etching the first and second masking materials using a chemical or mechanical process.

7. The method of claim 1 wherein depositing a second masking material on the substrate includes depositing the second masking material on the substrate with a first degree of anisotropy and wherein etching the second masking material from the substrate includes etching the second masking material from the substrate with a second degree of anisotropy being different from the first degree of anisotropy.

8. The method of claim 7 wherein depositing and etching the second masking material from the substrate with different degrees of anisotropy includes depositing the second masking material with a greater thickness in the vertical direction in an area adjacent to the first sidewall than the thickness of the second masking material in the first and second regions and uniformly etching the second masking material from the substrate in the vertical direction, thereby producing the second sidewall.

9. The method of claim 1 wherein selectively etching one of the first and second mask materials from the substrate includes performing the

etching using a chemical or mechanical process.

10. The method of claim 2 wherein spacing between the first channels is uniform.

11. The method of claim 2 wherein spacing between the first channels is non-uniform.

12. The method of claim 2 wherein forming a plurality of first channels in the substrate includes forming a plurality of structures in substrate separated by the first channels wherein the structures are spaced from each other by nanometer-scale dimensions and being of uniform thickness.

13. The method of claim 2 wherein forming a plurality of first channels in the substrate includes forming a plurality of structures in substrate separated by the first channels wherein the structures are spaced from each other by nanometer-scale dimensions and being of non-uniform thickness.

14. The method of claim 1 wherein the first and second sidewalls and the channels are spaced from each other by decananometer-scale dimensions.

15. A system including a plurality of multi-periodic, nanometer-scale semiconductor devices formed using the method of claim 1.

16. A plurality of multi-periodic, nanometer-scale electromechanical devices formed using the method of claim 1.

17. A method for forming a channel of nanometer-scale dimensions in a substrate, the method comprising:

(a) forming a first sidewall of first masking material on a substrate, the first sidewall having nanometer-scale width;

(b) depositing a second masking material on the substrate, such that the second masking material covers the first sidewall with a first thickness, forms second and third sidewalls on first and second sides of the first sidewall with a second thickness being less than the first thickness, and covers the substrate in regions adjacent to the second and third sidewalls with the first thickness;

(c) etching portions of the second and third sidewalls from the substrate such that the first and second sides of the first sidewall form discontinuities in the second masking material;

(d) removing the first sidewall from the substrate leaving a channel in the second masking material having substantially the same width as the first sidewall; and

(e) etching a channel in the substrate corresponding to the channel in the second masking material.

18. The method of claim 17 wherein forming a first sidewall of first masking material of nanometer-scale width on a substrate includes forming the first sidewall using edge definition lithography.

19. The method of claim 17 wherein etching portions of the second and third sidewalls from the substrate includes leaving deposits of the second masking material on the substrate having substantially uniform thickness in areas where the second and third sidewalls were present.

20. The method of claim 17 wherein etching portions of the second and third sidewalls from the substrate includes performing the etching using a chemical or mechanical process.

21. The method of claim 17 wherein removing the first sidewall from the substrate includes removing the first sidewall using a lift off method.

22. The method of claim 17 comprising forming a fourth sidewall of nanometer-scale dimensions in the channel.

23. The method of claim 22 comprising forming fifth and sixth sidewalls of nanometer-scale dimensions on opposite sides of the fourth sidewall to form a mushroom-shaped structure.

24. The method of claim 23 wherein the mushroom-shaped structure comprises a gate material for a semiconductor device.

25. A semiconductor device formed using the method of claim 24.

26. A semiconductor device formed using the method of claim 17.

27. The method of claim 1 wherein the substrate comprises a compound semiconductor material.

28. The method of claim 27 wherein the compound semiconductor material includes one of GaN, AlGaN, and InGaN.

29. The method of claim 1 wherein the substrate comprises a semiconductor heterostructure containing one of Si, GaAs, InGaAs, AlGaAs, SiGe, SiC, GaN, AlGaN, and InGaN.

30. The method of claim 1 wherein performing steps (a)-(e) includes forming the plurality of first channels in a first direction in the substrate and wherein the method further comprises repeating steps (a)-(e) to form a plurality of second channels in the substrate, the second channels intersecting the first channels at an oblique angle.

31. The system of claim 15 wherein the multi-periodic, nanometer scale devices include one of: a heterostructure field effect transistor (FET), a heterojunction bipolar junction transistor (BJT), a gallium-nitride-based FET, an indium-gallium-arsenide-based FET, a gallium arsenide FET, an indium-gallium-arsenide-based FET, and a gallium phosphide FET.

32. The method of claim 17 wherein the substrate comprises a compound semiconductor material.

33. The method of claim 32 wherein the compound semiconductor material includes one of GaN, AlGaN, and InGaN.

34. A semiconductor structure having an edge-defined, nanometer-pitched feature, the semiconductor structure comprising:

(a) a substrate comprising a first layer including a first semiconductor material and a second layer including a second semiconductor material, the first semiconductor material being different from the second semiconductor material; and

(b) at least one nanometer-pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography.

35. The semiconductor structure of claim 34 wherein the nanometer-pitched feature comprises a nanometer-pitched wall located on the first layer.

36. The semiconductor device of claim 35 wherein the nanometer-pitched wall is formed by a portion of at least one of the first and second layers.

37. The semiconductor structure of claim 34 wherein the nanometer-pitched feature comprises a nanometer-pitched channel formed in a masking material deposited on the substrate.

38. The semiconductor structure of claim 37 wherein the channel extends into at least one of the first and second layers.

39. A semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising:

(a) a semiconductor substrate;

(b) at least one micrometer-scale feature being located in or on the semiconductor substrate; and

(c) at least one nanometer-scale feature being located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography.

40. The semiconductor structure of claim 39 wherein the micrometer-scale feature comprises a channel or hole being defined by the substrate and the nanometer-pitched feature comprises a sidewall.

41. The semiconductor structure of claim 39 wherein the micrometer-scale feature comprises a mesa and the nanometer-scale feature comprises a sidewall located on top of the mesa.

42. The semiconductor structure of claim 39 wherein the micrometer-scale feature comprises a channel or hole being defined by the substrate and wherein the nanometer-scale feature comprises a channel located in a masking material deposited in the hole.

43. The semiconductor structure of claim 39 wherein the micrometer-scale feature comprises a mesa located on the substrate and wherein the nanometer-scale feature comprises a channel located in a masking material deposited on the mesa.

44. A field effect transistor having an edge-defined gate, the field effect transistor comprising:

(a) a substrate including a buffer layer of a first semiconductor material and a channel layer of a second semiconductor material, the second semiconductor material being different from the first semiconductor material; and

(b) a gate electrode being located on the substrate between the source and drain electrodes, the gate electrode being formed using edge definition lithography.

45. The field effect transistor of claim 44 wherein the substrate comprises a donor layer comprising a third semiconductor material being different from the first and second semiconductor materials, the donor layer including a channel, wherein the gate electrode is located in the channel.

46. The field effect transistor of claim 45 wherein the channel extends into the channel layer.

47. The field effect transistor of claim 44 wherein the channel layer includes a channel and the gate electrode is located in the channel.

48. The field effect transistor of claim 44 wherein the substrate includes a donor layer adjacent to the channel layer and the gate electrode is located on the donor layer.

49. The field effect transistor of claim 44 wherein the gate electrode is located on the channel layer.

50. A bipolar junction transistor having a nanometer-scaled edge-defined feature, the bipolar junction transistor comprising:

(a) a collector layer;

(b) a base layer being adjacent to the collector layer; and

(c) a nanometer-scale emitter being defined on the base layer using edge definition lithography.